

FIG 1

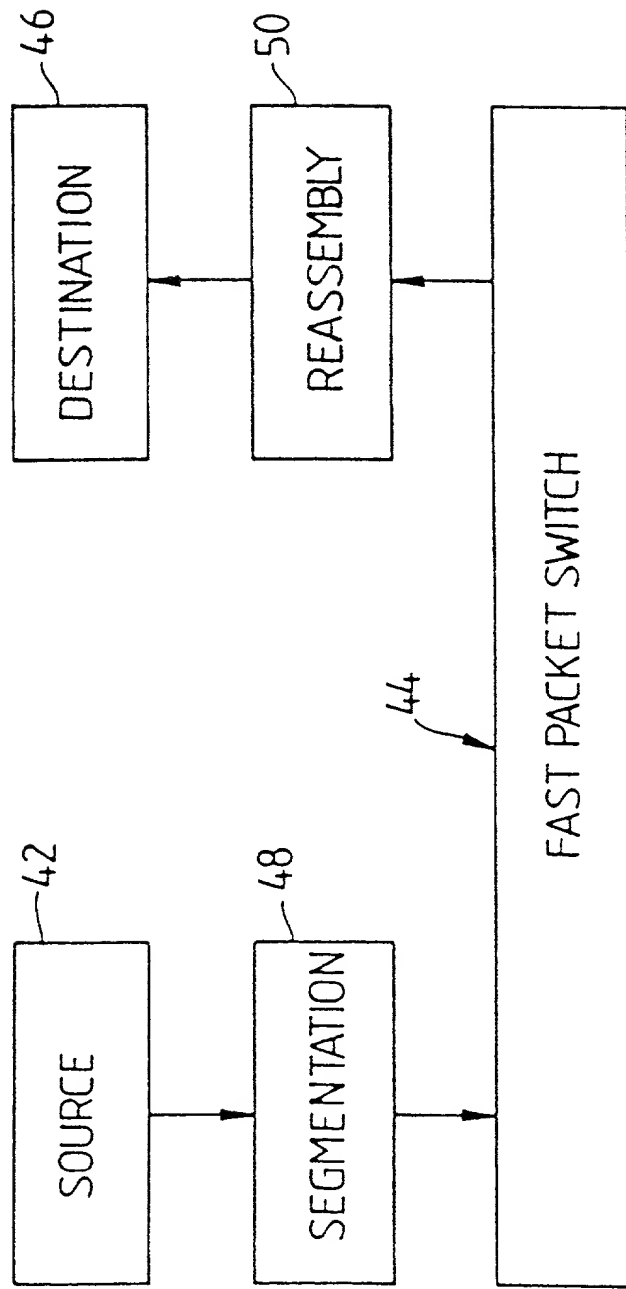
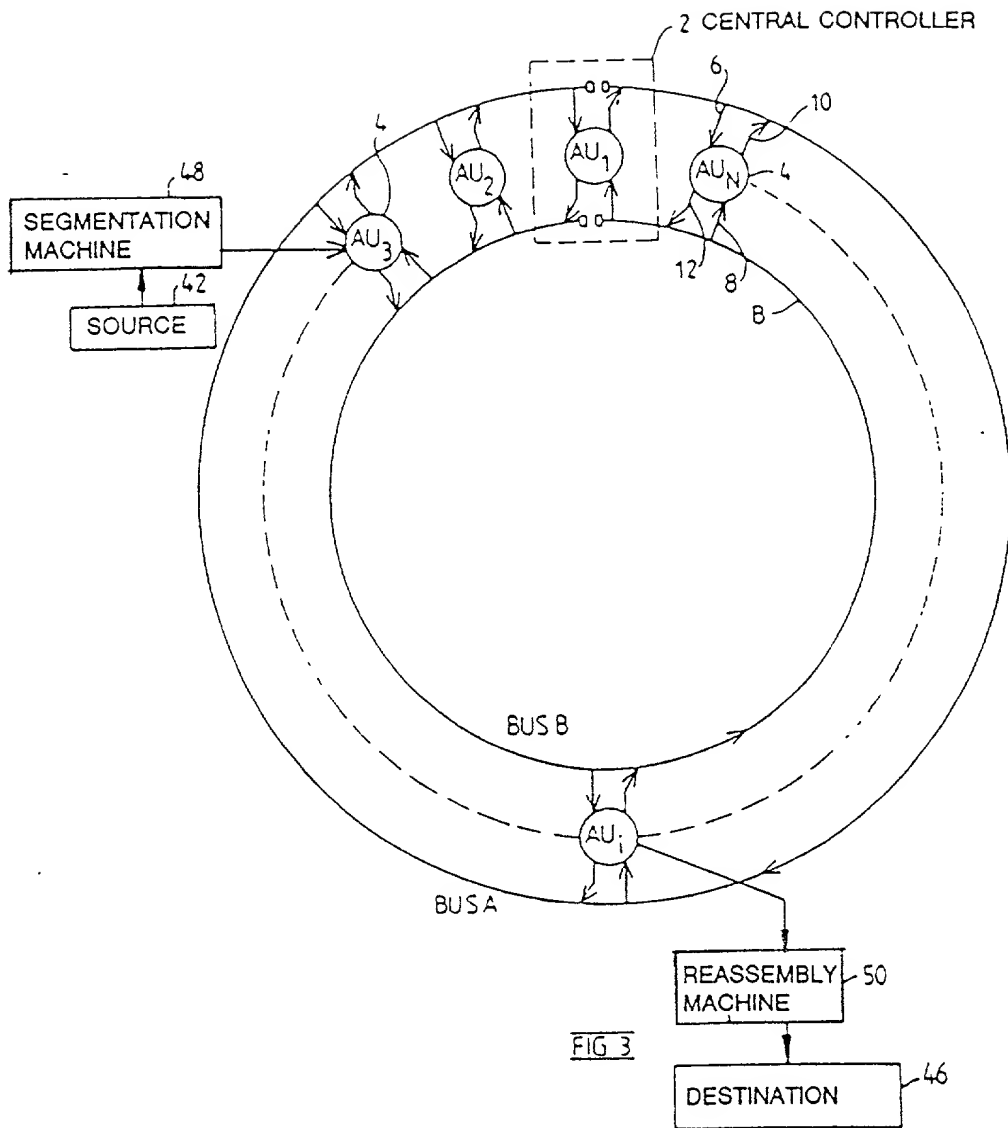


FIG 2

09010725.073401



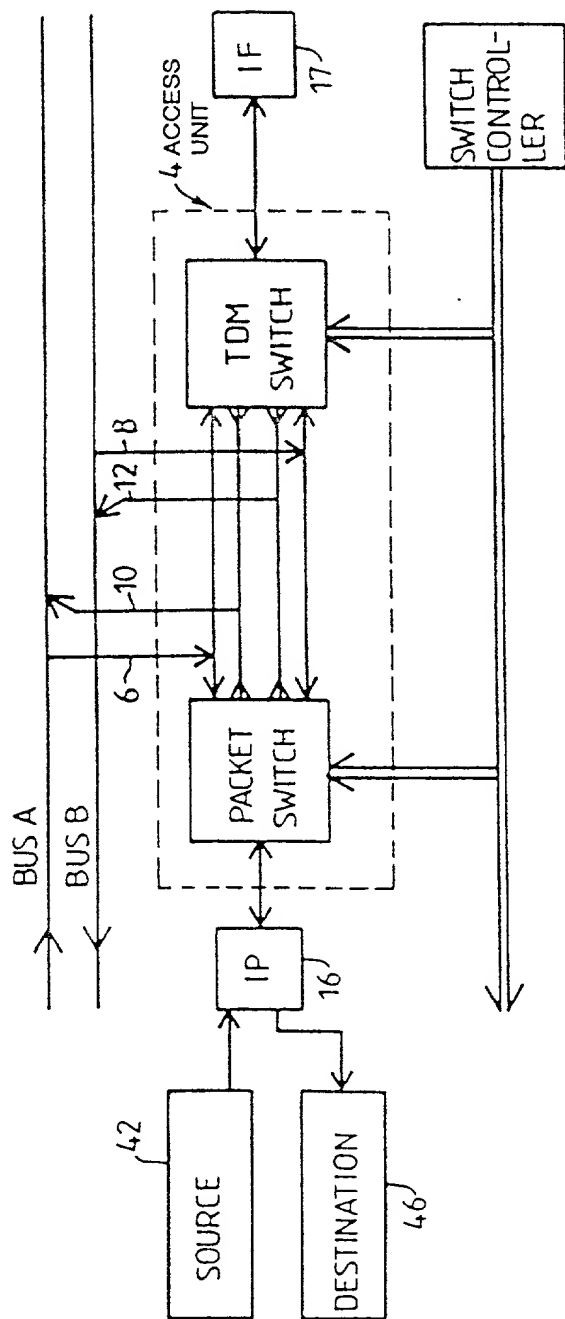


FIG 4

The diagram illustrates a data transfer system with two main processing blocks, one for each direction of data flow. The top block handles data from BUS A, while the bottom block handles data from BUS B. Both blocks contain a RECEIVE LOGIC (PV), BUFFER CONTROL, BUFFER, and DISTRIBUTED QUEUE LOGIC. They also feature S/P REG, FRAME SYNC, and P/S REG registers. Control signals like REQ, BUSY, and PO are used for coordination. A DELAY block is present in the lower path. The entire system is controlled by a CLK signal.

FIG 5

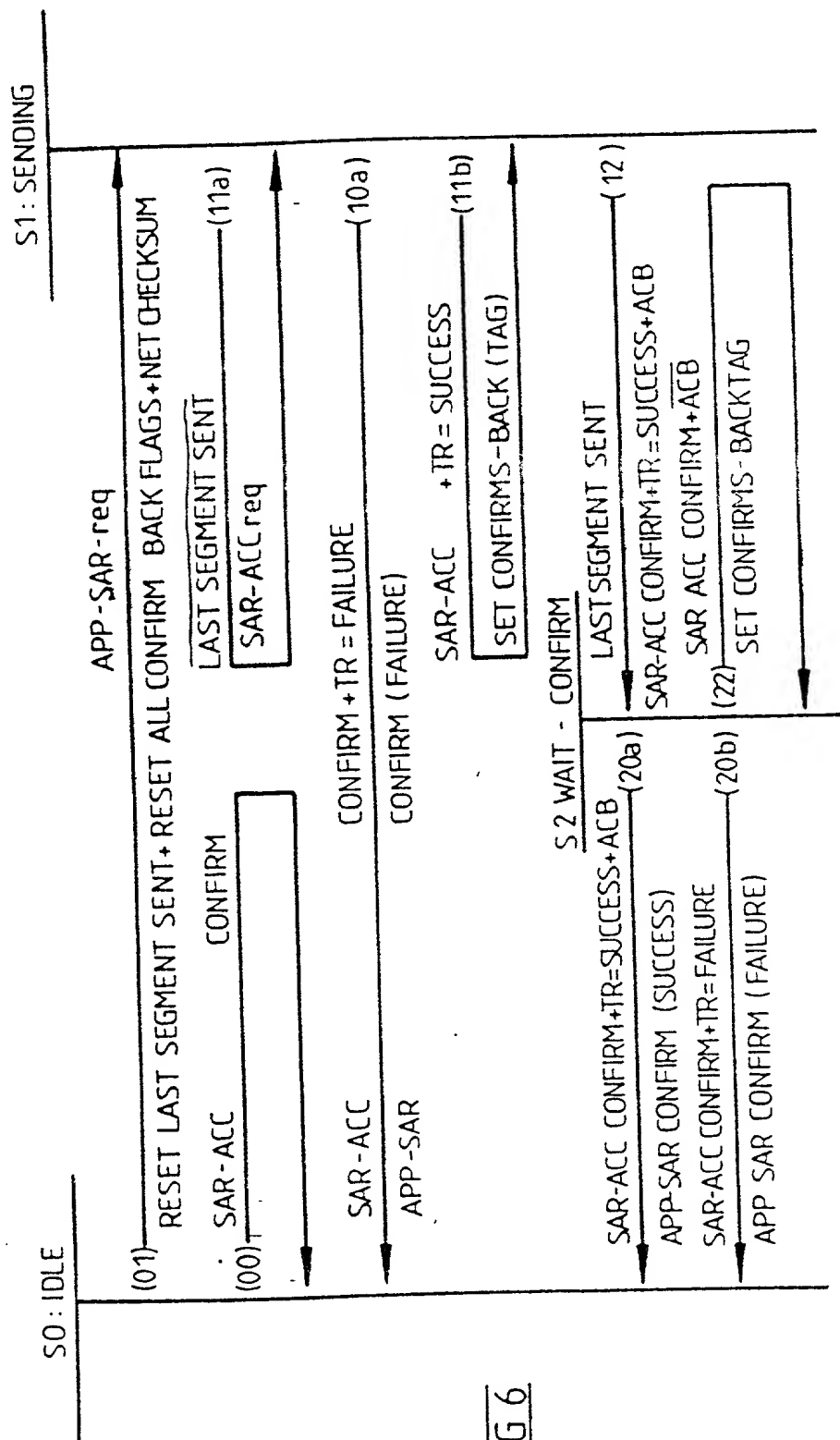


FIG 6

FIG 7

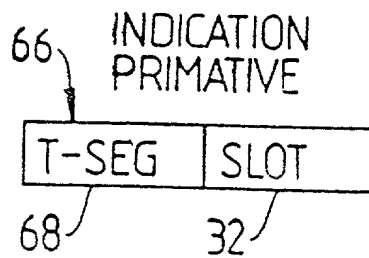
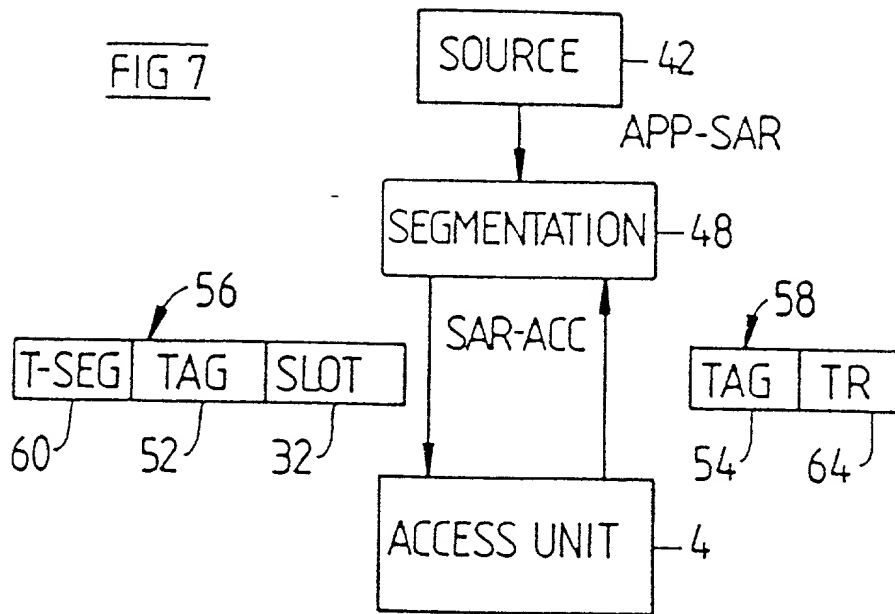
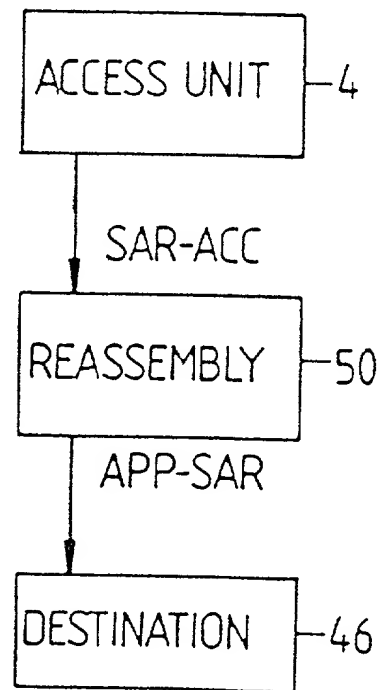


FIG 9



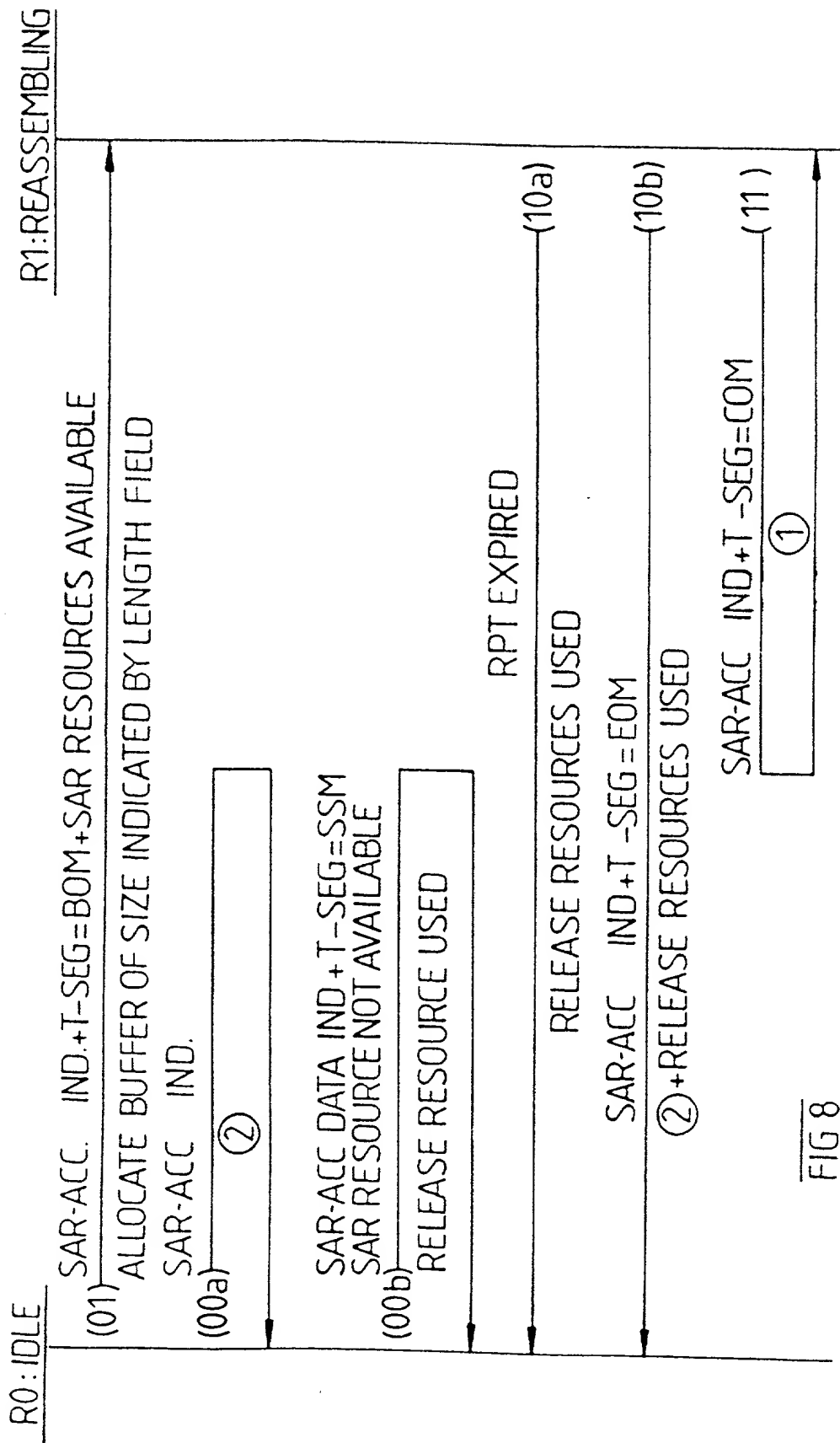


FIG 8



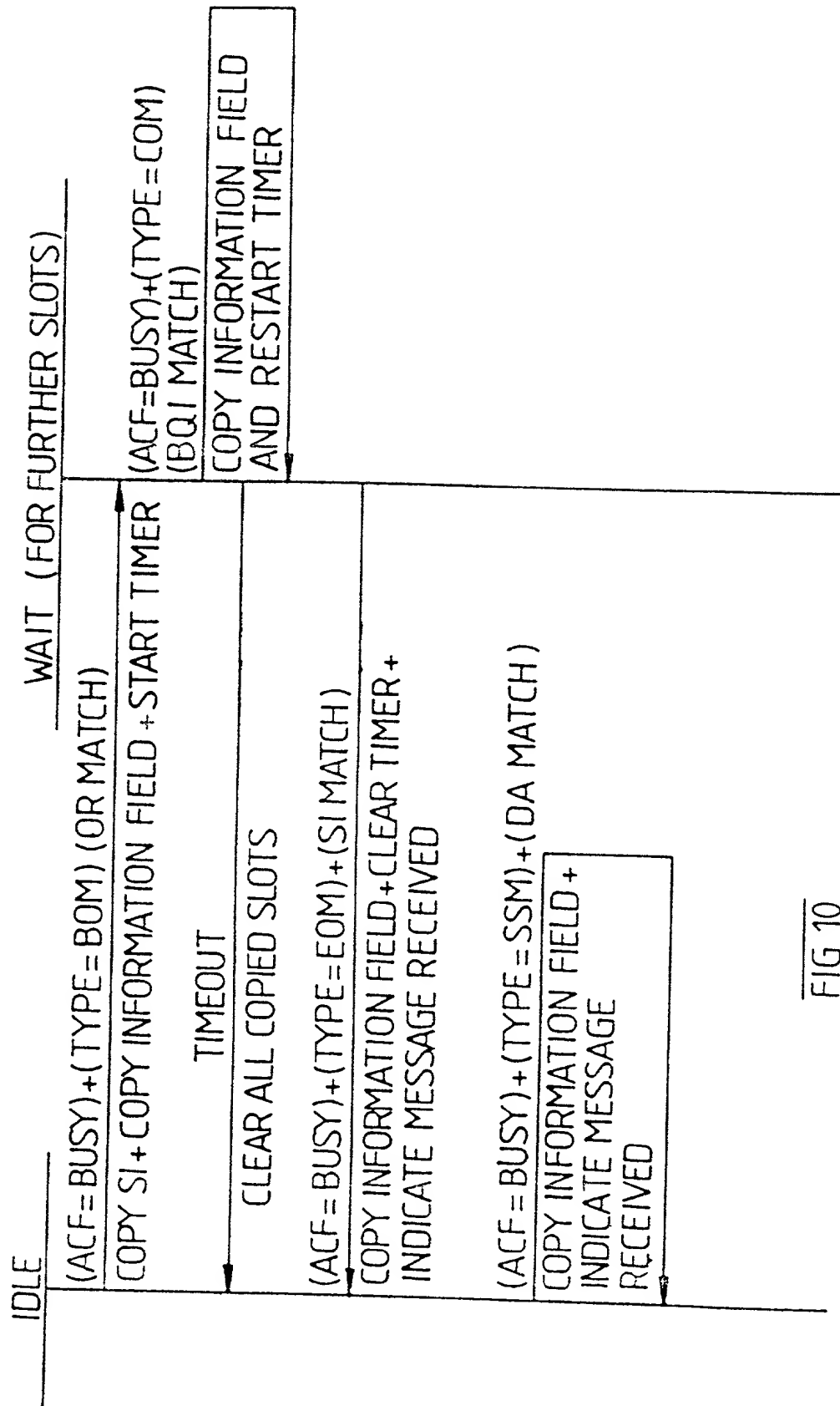


FIG 10

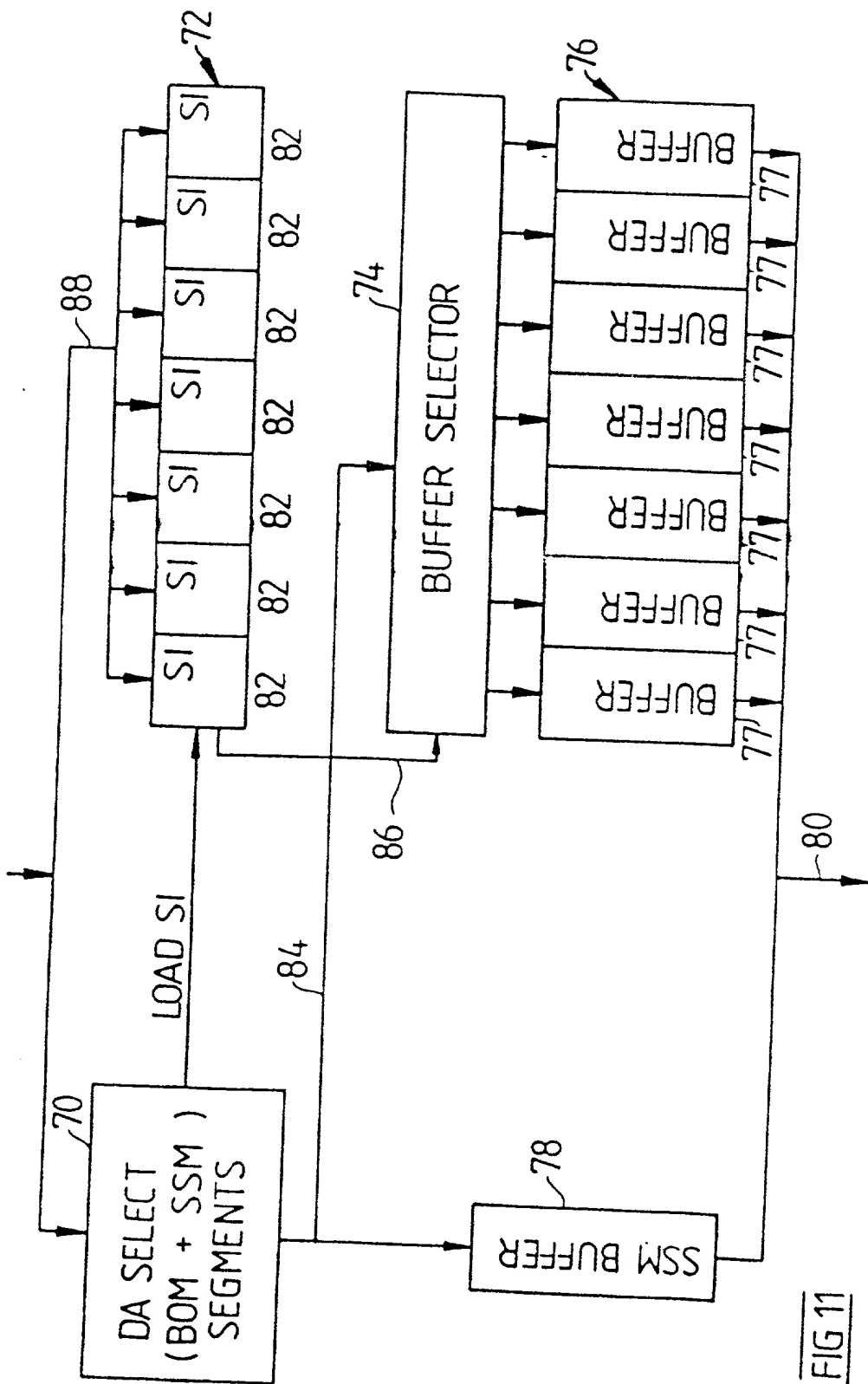


FIG. 11

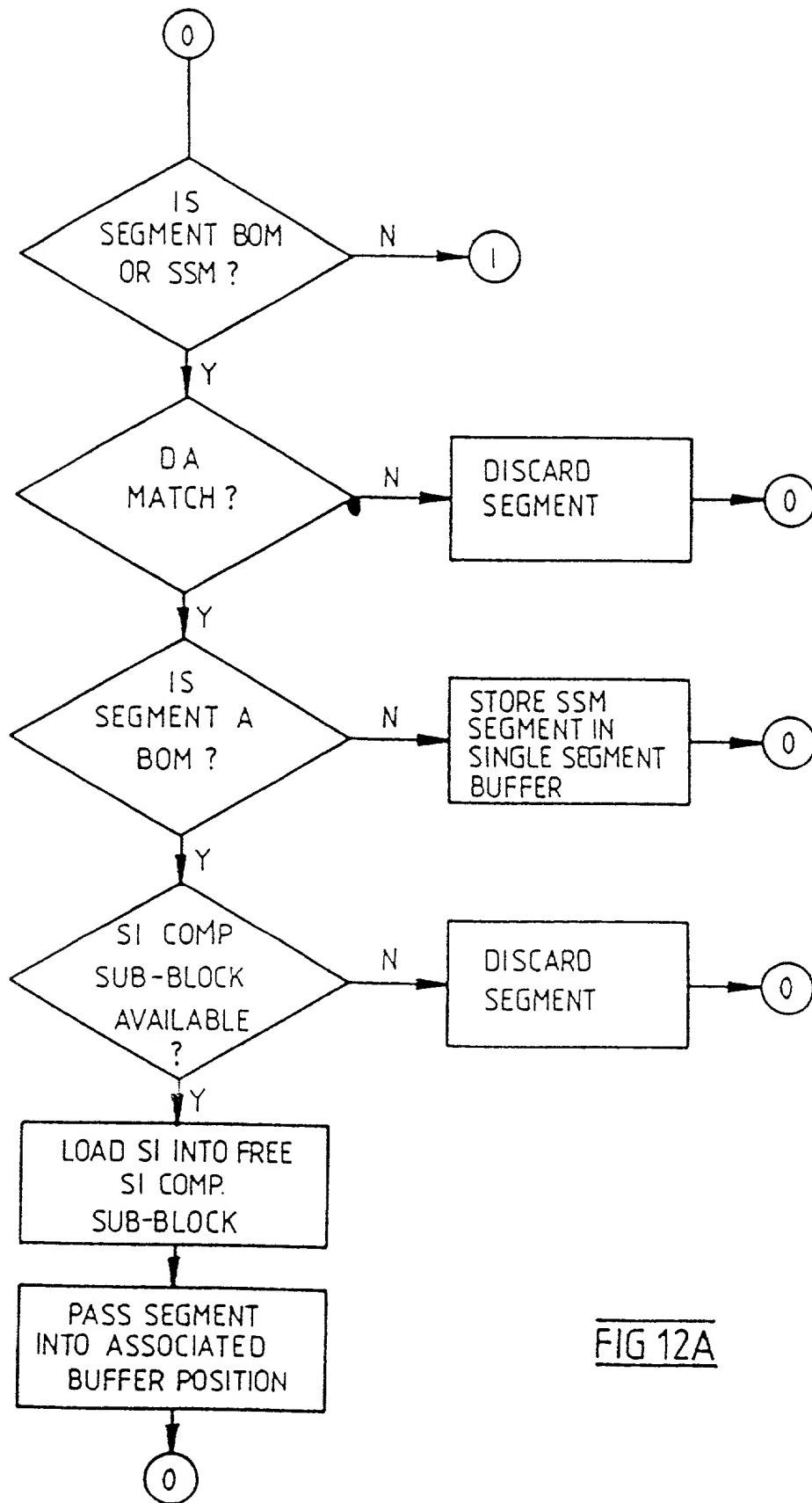


FIG 12A

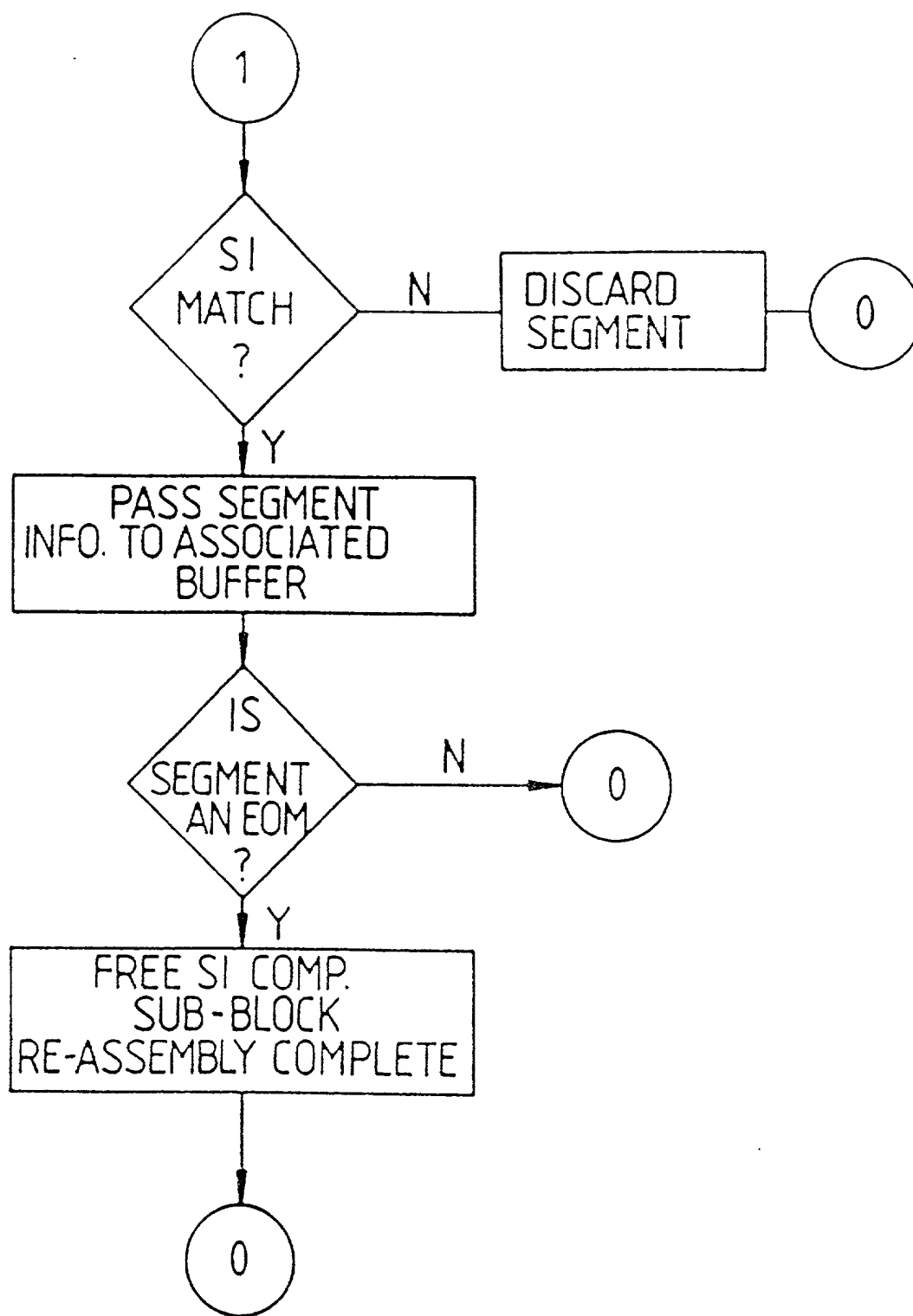


FIG 12B